REMARKS

This is a full and timely response to the outstanding non-final Office Action mailed July 30, 2004. Upon entry of the amendments in this response, claims 1-8, 10-17 and 19-31 remain pending. In particular, Applicants have amended claims 3, 5-8, 10-12, 14, 16, 19, 21, 23, 25, 27, 28, and 30. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Allowable subject matter

Applicants wish to place on record their appreciation of the Examiner for allowing claims 1, 2, and 29.

Objections to claims

Claim 3 is objected to because of the following informalities: The phrase "the PLL" is suggested to be changed to "a PLL." Claim 3 has been amended to eliminate this objection. Applicants respectfully request withdrawal of this objection.

Claim 10 is object to because of the following informalities: The phrase "claim 31" is suggested to be changed to "claim 3." Claim 10 was originally dependent on claim 9, which in turn was dependent on independent claim 7. In a previous response, claim 9 was deleted and claim 31 was added. Currently, claim 10 is dependent on claim 31, which in turn is dependent on independent claim 7. The dependency of claim 10 is proper and does not need correction. Applicants respectfully request withdrawal of this objection.

Rejection of claims under 35 U.S.C. §112

Claims 3-8, 10-17, 19-26, 28, 30, and 31 have been rejected under 35 U.S.C. 112, first paragraph, as allegedly failing to comply with the enablement requirement. Specifically, the Office Action states "[c]laims 3-8, 10-17, 19-26, 28, 30, and 31 recites the limitation "phase-locked loop" or "PLL" and goes on to explain that "the phase-locked loop (Fig. 7) from which this claim makes reference is actually not a loop."

As appropriate, Applicants have either removed the above discussed limitation or replaced it with the term "timing recovery circuit" from independent claims 3, 7, 11, 14, 16, 19,

21, 23, 25, 28, and 30 and dependent claims 5, 6, 8, 10, and 12. Applicants believe the modification eliminates the rejections and respectfully request withdrawal of these rejections.

The Examiner is respectfully requested to review the rejection of claim 13. Claim 13 is dependent on claim 1, does not contain the limitation discussed above, and has been allowable subject matter under previous office actions. Applicants believe claim 13 is allowable, and respectfully requests withdrawal of this rejection.

Rejections Under 35 U.S.C. §102

Claims 25 and 26 stand rejected under 35 U.S.C. §102(e) as allegedly being anticipated by Aslanis et al. (US Patent No. 5,627,863). Applicant respectfully traverses this rejection

For a proper rejection of a claim under 35 U.S.C. §102(e), the cited reference must discloses all elements/features/steps of the claim. See, e.g., *E.I. du Pont Nemours & Co. v. Phillips Petroleum Co.,* 849 F.2d 1430, 7 USPQ2d 1129 (Fed. Cir. 1988).

Independent Claim 25

Independent claim 25, as amended, is allowable for at least the reason that Aslanis does not disclose, teach, or suggest "a discrete Fourier transform (DFT) in communication with both the equalizer and the symbol synchronizer."

In this regard, and with reference to the teachings of the Aslanis patent, the Office Action has cited Fig. 1 and col. 5, lines 15-31:

> In the receiver 12, the signal received via the transmission path 18 is supplied by the hybrid circuit 16 to the filter and ADC unit 32, to reproduce the 544 serial samples per multicarrier symbol which are supplied to the time domain equalizer (TEQ) 34. The TEQ 34 is a finite impulse response filter which serves to limit most of the impulse response to less than the duration of the cyclic prefix, so that subsequent removal of the cyclic prefix reduces interference between consecutive multicarrier symbols. The equalized serial time domain sample stream is supplied to the buffer 36, which produces at its parallel output the 512 time domain samples of each multicarrier symbol, the 32 bits of the cyclic prefix thereby being removed. These 512 time domain samples are supplied to the 512-point FFT unit 38 and are transformed by this unit to a frequency domain multicarrier symbol, comprising 256 complex tone amplitudes, which is supplied to the frequency domain equalizer (FEQ) in the unit 40.

As can be verified from a review of these cited portions of Aslanis, there is no teaching or disclosure of "a discrete Fourier transform (DFT) in communication with both the equalizer and the symbol synchronizer." Aslanis merely discloses in Fig. 1 the output of TEQ 34 in communication with the input of buffer 36 (which is equated to the symbol synchronizer in the Office Action) and the output of buffer 36 in communication with the input of FFT 38. Therefore, even as defined in the Office Action, Aslanis discloses the symbol synchronizer in communication with the Fourier transform, but not the equalizer in communication with the discrete Fourier transform, and Aslanis does not disclose "a discrete Fourier transform (DFT) in communication with both the equalizer and the symbol synchronizer."

Accordingly, the rejection is deficient in this area. Notwithstanding, the undersigned has reviewed the entirety of the Aslanis patent and has failed to identify any such teaching anywhere within this reference. Accordingly, the Aslanis patent fails to teach or disclose the invention as defined by claim 25, and the rejection of claim 25 should be withdrawn.

Rejections Under 35 U.S.C. §103(a)

Claims 3-6 and 27 stand rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Aslanis et al. Applicants respectfully traverse this rejection.

It is well established at law that, for a proper rejection of a claim under 35 U.S.C. §103 as being obvious based upon a single reference, the reference must disclose, teach, or suggest, either implicitly or explicitly, all elements/features/steps of the claim at issue. *See, e.g., In Re Dow Chemical*, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and In re Keller, 208 U.S.P.Q.2d 871, 881 (C.C.P.A. 1981).

Independent Claim 3

Independent claim 3, as amended, is allowable for at least the reason that Aslanis does not disclose, teach, or suggest "applying the phase error directly to the ADC to modify the sampling timing of the ADC."

In this regard, and with reference to the teachings of the Aslanis patent, the Office Action has cited Fig. 1 and col. 6, lines 13-27:

> The receiver 12 includes a voltage controlled crystal oscillator (VCXO) 46 which produces on a line 48 a sampling clock signal for the ADC in the unit 32, synchronized to the 2.208 MHz sampling frequency of the transmitter 10 by a

> control loop which includes a phase comparator 50 and digital and analog control loop filters represented by a unit 52. The FEQ and decoder unit 36 supplies the phase information of the received pilot tone via a line 54 to the phase comparator 50, and a stored reference phase is also supplied to the phase comparator 50 from a store 56. The phase comparator 50 produces at its output a digital phase error control signal which is filtered by digital and analog filters in the unit 52 to produce an analog control voltage; this is used to control the VCXO 46 to maintain frequency synchronization.

As can be verified from a review of these cited portions of Aslanis, there is no teaching or disclosure of "applying the phase error directly to the ADC to modify the sampling timing of the ADC." Aslanis merely discloses "[t]he phase comparator 50 produces at its output a digital phase error control signal which is filtered by digital and analog filters in the unit 52 to produce an analog control voltage; this is used to control the VCXO 46 to maintain frequency synchronization." Therefore, Aslanis discloses that the phase error is filter and then applied to the VXCO, and Aslanis does <u>not</u> disclose "applying the phase error directly to the ADC to modify the sampling timing of the ADC."

According, the rejection is deficient in this area. Notwithstanding, the undersigned has reviewed the entirety of the Aslanis patent and has failed to identify any such teaching anywhere within this reference. According, the Aslanis patent fails to teach or disclose the invention as defined by claim 3, and the rejection of claim 3 should be withdrawn.

Independent Claim 27

Independent claim 27, as amended, is allowable for at least the reason that Aslanis does not disclose, teach, or suggest "means for applying the phase error to a timing recovery circuit to generate an output signal responsive to when a cyclic prefix is not present in the digital signal."

In this regard, and with reference to the teachings of the Aslanis patent, the Office Action has cited Fig. 1 and col. 6, lines 13-27:

> The receiver 12 includes a voltage controlled crystal oscillator (VCXO) 46 which produces on a line 48 a sampling clock signal for the ADC in the unit 32, synchronized to the 2.208 MHz sampling frequency of the transmitter 10 by a control loop which includes a phase comparator 50 and digital and analog control loop filters represented by a unit 52. The FEQ and decoder unit 36 supplies the phase information of the received pilot tone via a line 54 to the phase comparator 50, and a stored reference phase is also supplied to the phase comparator 50 from a store 56. The phase comparator 50 produces at its output a digital phase error control signal which is filtered by digital and analog filters in the unit 52 to

produce an analog control voltage; this is used to control the VCXO 46 to maintain frequency synchronization.

As can be verified from a review of these cited portions of Aslanis, there is no teaching or disclosure of "means for applying the phase error to a timing recovery circuit to generate an output signal responsive to when a cyclic prefix is not present in the digital signal." Aslanis merely discloses "[t]he phase comparator 50 produces at its output a digital phase error control signal which is filtered by digital and analog filters in the unit 52 to produce an analog control voltage; this is used to control the VCXO 46 to maintain frequency synchronization." Therefore, Aslanis discloses that the phase error is filter and then applied to the VXCO, and Aslanis does not disclose "means for applying the phase error to a timing recovery circuit to generate an output signal responsive to when a cyclic prefix is not present in the digital signal."

According, the rejection is deficient in this area. Notwithstanding, the undersigned has reviewed the entirety of the Aslanis patent and has failed to identify any such teaching anywhere within this reference. According, the Aslanis patent fails to teach or disclose the invention as defined by claim 27, and the rejection of claim 27 should be withdrawn.

Dependent Claims

Dependent claims 4-6; 8, 10, and 31; 15; 17; 20; 22; 24; and 26 are believed to be allowable for at least the reason that these claims depend from allowable independent claims 3; 7; 14; 16; 19; 21; 23; and 25, respectively. *In re Fine*, 837 F. 2d 1071, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

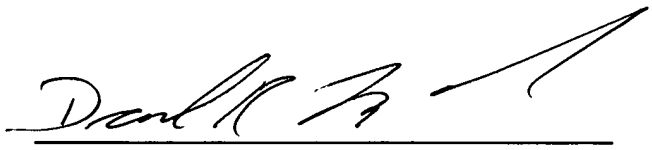
Cited Art Made of Record

The art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims 1-8, 10-17 and 19-31 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned representative at (770) 933-9500.

Respectfully submitted,



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